

App. Ser. No. 09/992,580
Atty. Dkt. No. MIO 0072 VA

REMARKS

Claims 23, 24, 52, 54, and 56 are pending in the present application. Claims 20, 53, and 55 have been cancelled. Claims 24 and 54 have been amended to correct the wording for securing the decoupling capacitor to the second stacking surface. Support for this amendment is found in Fig. 2 and in the specification at page 16, lines 4-11. In the specification, the Cross-References section has been updated. The Summary of the Invention has been amended to correctly describe securing the decoupling capacitor to the second stacking surface.

The Examiner rejected claims 54 and 56 under 35 U.S.C. §102(e) as being anticipated by Ball. According to M.P.E.P. § 706.02, in order to be anticipating under § 102, the reference must teach every aspect of the claimed invention. The Examiner has not shown that Ball teaches each and every aspect of the claimed invention. For example, referring to amended claim 54, the Examiner has not shown that Ball teaches “providing at least one conductive line connecting said decoupling capacitor, a bond pad on said second active surface, and a conductive contact on said first surface of said substrate.” The Examiner refers to Fig. 3 of Ball to teach a decoupling capacitor 82 secured to a second semiconductor die 54. However, Ball does not teach at least one conductive line connecting said decoupling capacitor, a bond pad on said second active surface, and a conductive contact on said first surface of said substrate. Instead, as can be seen in Fig. 3, Ball teaches a component 82 connected by a conductive line 88 to a contact 40 on the substrate 16. The component 82 is not connected to a bond pad on the second active surface 56 of the second die 54. Claim 56 is dependent on amended claim 54. Therefore, claims 54 and 56 are patentable over the cited and applied prior art.

The Examiner rejected claims 23, 24, and 52 under 35 U.S.C. §103(a) as being unpatentable over Hofstee et al. in combination with Spielberger et al. The Examiner has failed to establish a *prima facie* case of obviousness. According to the MPEP §706.02(j), to meet a threshold showing of *prima facie* obviousness, the Examiner must make three showings. The showings are: that there is some suggestion or motivation to modify the references; that there is a reasonable expectation of success; and that the prior art references teach or suggest all of the claimed limitations.

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The Examiner has not shown that there is some suggestion or motivation to combine Hofstee and Spielberger. The Examiner combines the prior art embodiment of Fig. 1 of Hofstee with the embodiments in Figs. 5 and 6 of Spielberger. The Examiner states that "it would have obvious to one of ordinary skill in the art to incorporate a decoupling capacitor to said second stacking surface in order to reduce propagation delays and transmission line effect as taught by Spielberger (Col. 1, Lines 38-39)."

Hofstee teaches a die packaging arrangement in which a die 106 and a die 104 are stacked such that the active surface of die 106 is coupled to the active surface of die 104, as shown in Fig. 1 (Paragraph 6). The die 106 is then connected to lead frame 114, and the dice are enclosed in a plastic or ceramic package 102 (Paragraph 6). Hofstee further teaches that a circuit 111 that is located at or near the center of the die must be connected to externally supplied power signals via a relatively long metallization interconnect 113 (Paragraph 7). Hofstee does not teach or suggest that additional components may be incorporated into the die packaging arrangement shown in Fig. 1.

Spielberger teaches a die arrangement wherein the active surface of the first die 20 faces the stacking surface of the second die 40. The decoupling capacitor 60 is secured to the active surface of the second semiconductor die, as shown in Figs. 5 and 6. There is no teaching or suggestion in Spielberger that a decoupling capacitor 60 be secured to a stacking surface such as that taught in Hofstee. The die stacking arrangements of Hofstee and Spielberger are not comparable. Instead, the scheme in Hofstee comprises an active surface of a first die secured to an active surface of a second die. Spielberger teaches an active surface of the first die facing the stacking surface of the second die.

Additionally, the Examiner has not demonstrated that Hofstee and Spielberger teach or suggest all of the claimed limitations. For example regarding claims 23 and 52, neither Hofstee nor Spielberger teach a decoupling capacitor secured to a second stacking surface. As discussed above, Spielberger does not teach at least one decoupling capacitor secured to a second stacking surface. Instead, the decoupling capacitor 60 is secured to the active surface of the second semiconductor die, as shown in Figs. 5 and 6. Hofstee does not teach a decoupling capacitor.

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In a further example, regarding claim 24, neither Hofstee nor Spielberger teach "electrically coupling said first active surface to said substrate with a plurality of topographic contacts extending from respective conductive bond pads on said first active surface to corresponding conductive contacts on said first surface of said substrate." As can be seen in Fig. 1 of Hofstee, the stacking surface of the die 106 would face a substrate. Similarly, as can be seen in Figs. 5 and 6 of Spielberger, the stacking surface of the first die 20 faces the substrate 16. Thus, neither Spielberger nor Hofstee teaches securing the active surface of the first die to a substrate. Thus, claims claims 23, 24, and 52 are patentable over the cited and applied prior art.

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CONCLUSION

Applicant respectfully submits that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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